A Case Study on Sequential Tripping Scheme

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***Abstract*—Tenaga Nasional Berhad is exploring the nonconventional method in dealing with fault current issues. Therefore, the intention of this paper is to present the results of a study which identifies and investigates the impact of the application of sequential tripping scheme, using a 275kV substation equipped with an out-door gas insulated switchgear as a study case. The study essentially attempts to identify potential concerns and explore suitable design, before finalizing the implementation solution for such scheme. Successful implementation of this scheme could save major cost by deferring the switchgear upgrading project to later date.**

Keywords—fault level; electromagnetic transient; gas insulated switchgear; sequential tripping; transient overvoltage

I. INTRODUCTION

Power system network topology is constantly changing as the economy grows and power consumption increases. With the growth of energy generation in tandem with the expansion of a closely knitted transmission networks, the increase in fault currents is something to be expected. Although it is as expected, these currents actually are able to adversely affect network installations by causing thermal and mechanical stresses, and ultimately can become highly destructive. Therefore, it is imperative for power utilities to reduce and control the fault currents.

One obvious remedy is to upgrade the equipment so that the equipment rating is considerably higher than the estimated fault current. This approach usually involves complete rebuilding of a substation. However, sometimes this approach is something that can not be justified from an economic standpoint. Other operational method of reducing fault level, by means of busbar splitting or open point, is not acceptable for a grid system that requires high interconnectivity for power transfer flexibility, hence grid reliability. Tenaga Nasional Berhad Malaysia (TNB) is facing similar problem with its transmission system. As such, TNB is exploring the nonconventional method in dealing with fault current issues.

II. OBJECTIVE

The fault current at Substation Y is expected to exceed its circuit breaker breaking capacity by year 2013[1]. Substation Y is a 275kV substation equipped with an out-door gas insulated switchgears (GIS) rated at 31.5kA for 3 seconds. One option to mitigate this problem is by installing current limiting reactor. However, this solution is not favorable due to implementation challenges and high losses incurred throughout the operation years.

Cursory analysis concluded that one of the most plausible solutions would be applying the sequential tripping scheme to isolate faults. Therefore, the objective of this paper is to present the results of a study which identifies and investigates the impact of the application of sequential tripping scheme using Substation Y as a study case. The ultimate goal of this study is basically to identify potential concerns and explore appropriate design, prior to finalizing the solution for Substation Y.

Fig. 1. Outdoor GIS at Substation Y

III. MOTIVATION

In many cases, in addition to network splitting, the traditional way of solving fault current issues in TNB has always been physical upgrading of a substation. Therefore, to mitigate high fault current in Substation Y and to comply with the stipulated criteria, Substation Y was proposed to be upgraded to meet the fault current requirement by year 2013.

Substation Y was commissioned in 1988. For this GIS type of switchgear, the average service life is 40 years[2]. Normally, under these circumstances, Substation Y will be upgraded despite still having 15 years of its remaining service life. This will be a squander of capital because Substation Y is still in a good condition and is operating faultlessly.

In many other utilities, other than physical upgrading of equipment, various measures have been explored and implemented to achieve the same objective. One particular approach defined by the IEEE and EPRI is sequential tripping scheme of the circuit breakers to manage high fault current

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using the existing circuit breakers [3,4]. With this method, the useful life of the existing switchgear can be prolonged, thus resulting in huge cost saving. At the same time, it avoids the complexity of the outage management. The successful implementation of sequential tripping scheme at Substation Y could save major cost to TNB by deferring the switchgear upgrading project to a later date.

IV. LITERATURE REVIEW

Fault current is the current flow during a short. Commonly also being referred to as "short-circuit current". It passes through all the electrical paths in the affected circuit. The faults or "short", may take various forms such as three-phase short circuit, one-phase to ground short, two-phase short circuit, two-phase to ground short, one-phase break, two-phase break or even complex faults.

Generally, the magnitude of fault current is large and, therefore, hazardous. The primary problems with high fault currents were explained by [5] as:

- The system throughout and any equipment which the fault current flows, will be subjected to high mechanical dynamic stress due to electromagnetic forces. In order for equipment to withstand these stresses, an adequate mechanical reinforcement is required.
- High thermal stresses, particularly if arcing occurs.

It is physically difficult to interrupt high current. It raises the need for a sophisticated mechanical contact system, e.g. circuit breakers[6].

Reference [7] discussed various fault current limiting measures currently in use by utility companies. As illustrated in Fig. 2, these measures can be categorized into two sets of categories:

- "Passive" – Impedance increase, which can be permanent or condition based, and
- "Active" – Primarily an apparatus measures.

Passive technique offers attractive solution where fault current can be reduced by mean of increasing the source impedance. Examples of passive technique are grid splitting or off points, connecting generation at higher voltage levels, and design of specific equipment of power system components, e.g. high impedance transformers and series reactors. Passive technique does not require external triggering. Under system fault condition, it will alter the source impedance by naturally inserting its impedance[8].

Alternatively, there are so-called "active" devices that provide utility companies additional options to lessen the prospective current that flows whenever there is a fault. Examples of active fault current limiting devices are:

- Pyrotechnic I_S Limiters or fuses; commercially available for up to medium voltage application[9],
- Solid-state fault current limiting circuit breakers,
- Superconducting fault current limiters; prototype under testing for application up to 138kV[10],
- Inter-phase power controllers, and
- Active fault level management

Fig. 2. Overview of Fault Current Limiting Measures[5]

As discussed in [5], under normal system operating conditions, all of the devices effectively exhibit small impedance property. These devices will increase the impedance only during fault conditions. These active devices, however, require active triggering. As such, they may even fail to operate that, consequently, they do not produce current limiting action.

A. *Sequential Tripping*

The sequential switching is a method by which the "multiple sources contributing to any fault current are separated prior to the clearance of the faulted section"[11]. Sequential Tripping Scheme offers the cheapest and fastest alternative, yet technically feasible solution. This section explores the principle of Sequential Tripping and highlights the pros and cons of this scheme.

The IEEE defines sequential tripping as "the tripping of breakers in pre-determined sequence"[3]. EPRI further refines the definition as "sequential tripping of circuit breakers is a special measure occasionally used in substations to manage high fault currents without replacing all circuit breakers"[4]. In summary, sequential tripping is a scheme to prevent circuit breakers from interrupting excessive fault current.

As illustrated in Fig. 3, two separate fault current components collectively contribute to the total fault current from the source, namely through transformer T1 and T2. Under normal circumstances, circuit breaker CB-5 would be tripped in the occurrence of a fault downstream falls within its protection zone.

However, with the system growing over the years, the total fault current surging through CB-5 exceeds its breaking capacity. In this case, tripping of CB-5 can be inhibited until either breaker CB-1, CB-2 or CB-3 operates first. This

effectively removes a component of the fault current and reduces it to within CB-5's zone of protection at the fault's location. Breaker CB-5 then, can be opened safely. With this approach, the capital expenditure to upgrade CB5 can be deferred, especially if the circuit breaker has not reached the end of its technical/economic life.

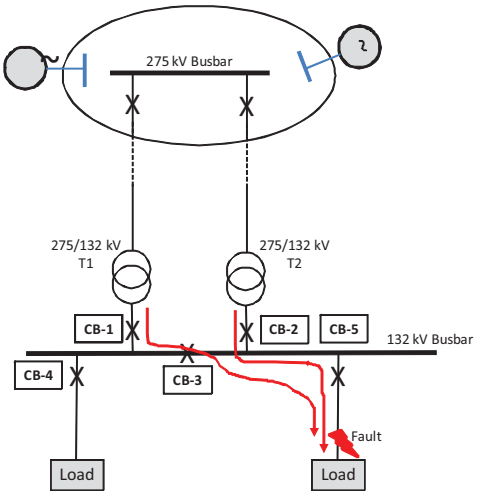

Fig. 3. The Concept on Sequential Tripping

Sequential tripping scheme offers the cheapest and fastest alternative solution. Similar to inserting Series Current Limiting Reactor, this option requires no change to the existing substation. One example of successful implementation of sequential tripping scheme is in one of the 138kV substations in American Electric Power (AEP) grid network[12].

B. *Issues on Sequential Tripping*

Nevertheless, like all other options, there are concerns that need to be addressed if such scheme is to be adopted. The issue associated with sequential tripping, particularly with GIS, is the large number of re-strike or prestrike between the contacts. Re-strike or prestrike may occur during closing or opening operation of GIS disconnector[13]. Each strike leads to generation of a transient overvoltage (TOV). The TOV has very fast rise-times, in the range of a few nanoseconds, and is proceeded by high frequency oscillations. The TOV magnitude depends on the substation layout, magnitude of the trapped charge on the high voltage (HV) bus as well as the location of the switching point[14]. In sequential tripping scheme, one will expect a minimum of one successive switching at different switching points. Thus, it is essential to study the successive switching effect on the TOV magnitudes.

Another major issue concerning sequential tripping is the total fault clearing time. Typically, when a fault is detected, the time taken to clear the fault is about 95 milliseconds. The total operating time consists of the current transformer's time constant, relay operation time, master trip, breaker operating time and arc quenching time. Under the scenario of which two circuit breakers operating consecutively, the fault clearing time is longer. Thus, it is imperative to ascertain that the system is robust to tolerate a longer fault clearing time.

V. APPROACH & METHODOLOGY

A. *General Approach*

Conceptually, the proposed sequential tripping scheme comprises an intelligent protection and control scheme with fault detection and discriminator, a strategic computation and a sequential execution sub-system. Its objective is to systematically choose the right circuit breakers and their sequences to trip in an event of high fault current exceeding the faulted equipment short circuit rating. The system needs to determine the source, the split and the faulted circuits and performs on-line calculation to determine the appropriate tripping sequence.

B. *Methodology*

The study was divided into three parts: Part I is the steady state analysis; Part II looks into transient stability; and Part III is the electromagnetic transient study that will examine the issue associated with Sequential Tripping Scheme, particularly the TOV.

1) Part I: The steady state analysis involves detailed modelling of Substation Y and short circuit analysis. It is to determine the common sequence to trip the circuit breakers under all possible combination of fault events. The short circuit assessment is an extension of a load flow analysis whereby faults are simulated at various parts of the system to identify the fault levels. The short circuit performance is to be benchmarked against the criteria stated by relevant clauses of the Transmission System Reliability Standards (TSRS)[15].

In a steady state load flow and short circuit analysis, a substation can be modeled either as a nodal topology, or detailed (or elementary) topology. In the nodal topology, a substation can be modeled as a single electrical node and the branches of which are the transmission system components (lines, cables, transformers), connected to it. In TNB's normal practice in load flow and short circuit calculations, the system is represented in the nodal topology.

In the detailed topology, on the other hand, a substation is represented with its switching equipment (circuit breakers, isolators), busbar section, busbar connection, etc[16]. It can be represented by a collection of equipments, in which the nodes are the internal connections, and the branches represent the switching devices in the closed position. It is assumed that all elements of a connected part have the same voltage, which means that the impedances of the elements can be neglected.

Substation Y was modeled in detailed topology, using PSS/E Software, with bus coupler and busbar to reflect the fault current that flows through each breaker. Only the three phase to ground solid zero-impedance fault was considered. Fault currents flowing through each circuit breaker was studied for the following fault conditions under all possible circuit connection permutations:

- Bus Fault, and
- Close-in Line-end Open Fault

Detailed topology permits individual breaker analysis to be performed consistent with Substation Y breaker arrangement.

2) Part II: Part II is a full-scale transient stability analysis. It requires the establishment of a full system dynamic model. The stability assessment would encompass the following types of simulation studies:

- Establishment of system fault clearing times, i.e. maximum fault duration before the generators run out of step (i.e. rotor angular difference exceeding 180 degrees). The maximum fault clearing time derived from this part of the study can be used as an input to the design of sequential tripping schemes for Substation Y.
- Performance of the system with respect to various types of faults at key transmission buses, Substation Y in particular, with both normal and extended fault clearing times. This includes the auto-reclose operation on overhead line faults
- System response to beyond criterion contingency, such as total loss of a substation.

The performance of system responses is to be benchmarked against the criteria stated by relevant clauses of the TSRS.

3) Part III: This is the electromagnetic transient study. The study involves development of detail modeling of transmission components including the insulators, current transformers, isolators, circuit breakers, protective relays etc. For this purpose, information gathering shall include the current status and ratings of relevant equipment at Substation Y. Some tripping test may be conducted to ensure proper modeling for the study.

The response of full AC system is to be represented by employing appropriate modeling techniques, including the use of network equivalence. However, the system response using "equivalent network" needs to be verified accordingly before proceeding with the detailed studies.

The electromagnetic transient studies shall include, but not limited to:

- Transient Switching Overvoltage (TOV) studies to determine the worst over voltages and maximum energy that the existing surge arrestor has to endure during various switching operations and faults in the system.
- Breaker transient recovery voltage (TRV) studies to determine the breaker interrupting capability in clearing various type and location of faults.

VI. STUDY RESULTS

A. Steady State

The layout of Substation Y is depicted in Fig. 4. The substation is of a double busbar arrangement with a single bus coupler. The substation comprises six feeders from Station L, Station M and Station N; and four units of 275/132kV Transformers. The circuit breakers are rated at 31.5kA for 3 seconds.

Employing the New York Independent System Operator (NYISO) guidelines in calculating the short circuit current[17], under the worst case condition, the fault level at Substation Y can reach a maximum of 40kA. Individual breaker analysis shows that, except for the bus coupler, all other breakers would be over duty when subjected to a bus fault and close-in line-end open fault. One way to solve this problem is by employing sequential tripping scheme.

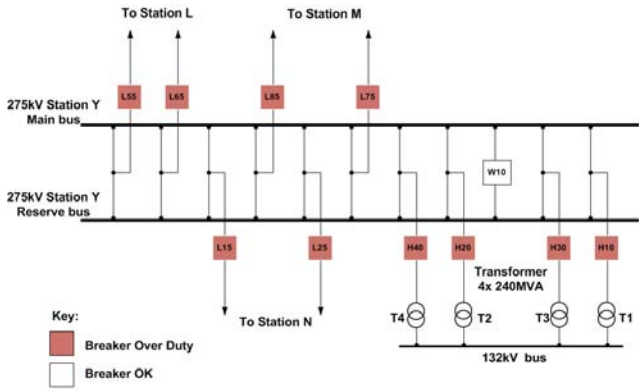

Fig. 4. Elementary Topology of Substation Y

1) Arming Logic: Reliability is the utmost importance in the operation of a grid system. As such, the Sequential Tripping Scheme for Substation Y should be designed such that it would operate only when fault level at Substation Y exceeds the circuit breaker rating of 31.5kA. In all other condition, the scheme has to be deactivated to avoid unnecessary operation.

A truth table consisting of the status of all six feeders from Station L, Station M and Station N, was tabulated to determine whether or not the scheme needs to be activated i.e. when the fault level exceeds 31.5kA. As shown in Table I, only certain combination of line breaker status necessitates scheme activation.

The result from the Truth Table serves as an input to the Karnaugh Map shown in Fig. 5. The map provides simple and straight forward method of minimizing Boolean expressions. Employing this technique, the Boolean Function to activate the Sequential Tripping Scheme for Substation Y is;

$$z = A{\cdot}E + B{\cdot}E + C{\cdot}E + D{\cdot}E + A{\cdot}F + B{\cdot}F + C{\cdot}F + D{\cdot}F \quad (1)$$

$$z = E{\cdot}(A + B + C + D) + F{\cdot}(A + B + C + D) \quad (2)$$

where z is the output whether or not to activate the scheme, and A, B, C, D, E, and F are the respective breaker ON/OFF status.

The logical expression can be further translated into a Logic Circuit as depicted in Fig. 6. The tripping sequence is tested for all condition with status "z = 1" as indicated in Table I.

TABLE I. POSSIBLE LINE BREAKER STATUS AGAINST FAULT EXCEEDING BREAKER DUTY

sequence	Input: Line Breaker						output
	L15	L25	L55	L65	L75	L85	
	A	B	C	D	E	F	z
0	0	0	0	0	0	0	**0**
1	0	0	0	0	0	1	**0**
2	0	0	0	0	1	0	**0**
3	0	0	0	0	1	1	**0**
4	0	0	0	1	0	0	**0**
5	0	0	0	1	0	1	**X**
6	0	0	0	1	1	0	**X**
7	0	0	0	1	1	1	**1**
8	0	0	1	0	0	0	**0**
9	0	0	1	0	0	1	**X**
10	0	0	1	0	1	0	**X**
11	0	0	1	0	1	1	**1**
12	0	0	1	1	0	0	**0**
13	0	0	1	1	0	1	**1**
14	0	0	1	1	1	0	**1**
15	0	0	1	1	1	1	**1**
16	0	1	0	0	0	0	**0**
17	0	1	0	0	0	1	**1**
18	0	1	0	0	1	0	**1**
19	0	1	0	0	1	1	**1**
20	0	1	0	1	0	0	**0**
21	0	1	0	1	0	1	**1**
22	0	1	0	1	1	0	**1**
23	0	1	0	1	1	1	**1**
24	0	1	1	0	0	0	**0**
25	0	1	1	0	0	1	**1**
26	0	1	1	0	1	0	**1**
27	0	1	1	0	1	1	**1**
28	0	1	1	1	0	0	**0**
29	0	1	1	1	0	1	**1**
30	0	1	1	1	1	0	**1**
31	0	1	1	1	1	1	**1**

sequence	Input: Line Breaker						output
	L15	L25	L55	L65	L75	L85	
	A	B	C	D	E	F	z
32	1	0	0	0	0	0	**0**
33	1	0	0	0	0	1	**1**
34	1	0	0	0	1	0	**1**
35	1	0	0	0	1	1	**1**
36	1	0	0	1	0	0	**0**
37	1	0	0	1	0	1	**1**
38	1	0	0	1	1	0	**1**
39	1	0	0	1	1	1	**1**
40	1	0	1	0	0	0	**0**
41	1	0	1	0	0	1	**1**
42	1	0	1	0	1	0	**1**
43	1	0	1	0	1	1	**1**
44	1	0	1	1	0	0	**0**
45	1	0	1	1	0	1	**1**
46	1	0	1	1	1	0	**1**
47	1	0	1	1	1	1	**1**
48	1	1	0	0	0	0	**0**
49	1	1	0	0	0	1	**1**
50	1	1	0	0	1	0	**1**
51	1	1	0	0	1	1	**1**
52	1	1	0	1	0	0	**0**
53	1	1	0	1	0	1	**1**
54	1	1	0	1	1	0	**1**
55	1	1	0	1	1	1	**1**
56	1	1	1	0	0	0	**0**
57	1	1	1	0	0	1	**1**
58	1	1	1	0	1	0	**1**
59	1	1	1	0	1	1	**1**
60	1	1	1	1	0	0	**0**
61	1	1	1	1	0	1	**1**
62	1	1	1	1	1	0	**1**
63	1	1	1	1	1	1	**1**

Key:
Input
1: fault exceeds breaker duty
0: fault within breaker duty

Output
1: Activate Scheme
0: Deactivate Scheme
X: Don't care

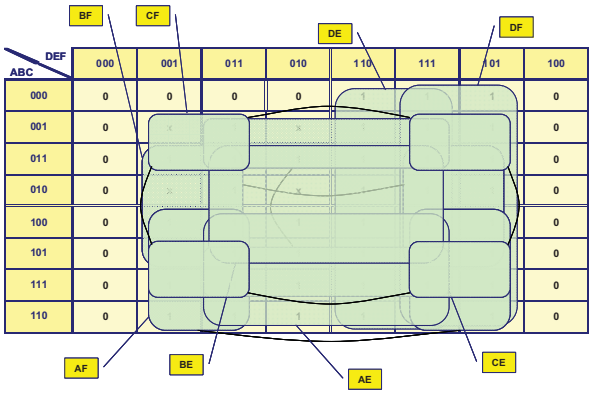

Fig. 5. Karnaugh Map for Switching Sequence's Boolean Expression

2) Tripping Sequence: Once the logic to activate the scheme has been decided, the next step is to determine the most common sequence to trip the breakers to clear the fault. Analysis indicates that the most common sequence to trip the breakers is L75, L85, followed by the breaker of faulted element. If the fault occurs near breaker L75, exemption has to be made such that L85 is to be tripped first.

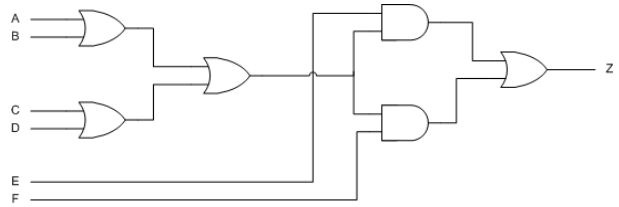

Fig. 6. Sequential Tripping's Arming Logic for Substation Y

It is also observed that for any busbar fault, the fault current flowing through each breaker is within the breaker duty. Therefore, it is safe to open all breakers and the scheme can be defeated.

B. *Transient Stability*

System stability is another concern with the delayed clearing time. In the proposed scheme, breaker L75 and L85 will be tripped simultaneously, followed by tripping of the breaker of faulted element at its primary zone of protection. The total fault clearing time is therefore summed up to 145 milliseconds. Simulations confirmed that the system remains stable with the implementation of sequential tripping scheme. Fig. 7 shows the plot of relative rotor angle of the machines during the operation of the sequential tripping.

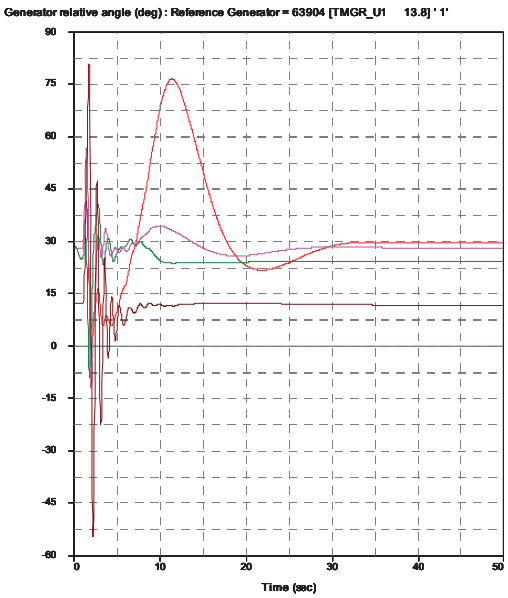

Fig. 7. Machines Relative Rotor Angle under Worst Case Scenario

C. *Electromagnetic Transient*

The electromagnetic transient study was performed entirely using PSCAD software, where PSS/E network data was used to create a simulation model in PSCAD (*.psc) after ETRAN software converted PSS/E *.raw files into an equivalent network after network reduction is applied. A network reduction is necessary here because otherwise the modeling requirements for simulating the whole network may be too

cumbersome to implement, e.g. excessive simulation time, risk of numerical instability, etc.

For this study, the critical TOV investigated was the circuit breaker's TRV for all breakers involved in the fault clearing sequence. For comparison purposes, both conventional and sequential protection tripping schemes were evaluated to quantify the risk from such switching transients based on IEC 56-1987 Standard[18]. Test Duty 4 (100% breaking current) of the IEC 56-1987 was specifically used to check withstand capability of the circuit breakers at Substation Y.

The most onerous conditions and system parameters were selected to optimize the required simulation cases and yield sufficient results to give the required verdict. Major elements in Substation Y were modeled as detailed as necessary, particularly taking into account GIS portion by using Frequency Dependent Phase Model. All type of faults were simulated using bolted and resistance faults for short line fault (SLF).

The conventional tripping scheme trips out the circuit breaker of the faulted feeder at Substation Y and the simplified control logic is as follows:

Fig. 8. Simplified control logic for conventional tripping

On the other hand the sequential protection tripping scheme trips out two pre-defined source side feeder circuit breakers (say L75 and L85) prior to tripping the circuit breaker of the faulted feeder. Similarly, the simplified control logic is as follows:

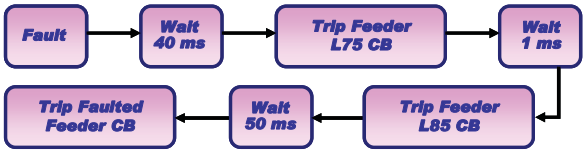

Fig. 9. Simplified control logic for sequential tripping

In term of fault current magnitude, Fig. 10 and Fig. 11 depicted the waveforms of fault currents as seen at the fault feeders using both conventional and sequential protection tripping schemes, respectively.

With the conventional tripping, the fault currents at the fault feeder remain high, approximately 40 kA, prior to tripping. This value is way beyond the breaker's breaking capacity. On the contrary, when the sequential tripping scheme was employed, the fault currents at the faulted feeder are lower, approximately 25 kA, prior to tripping. This is a promising evidence that the sequential switching scheme is working as what it is intended for.

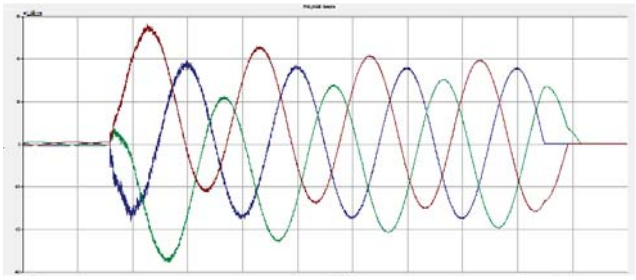

Fig. 10. Conventional protection tripping (grounded three phase SLF) – Fault currents at the fault feeder remain high (approximately 40 kA) prior to tripping.

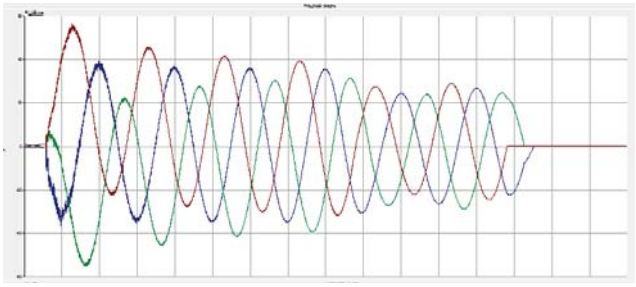

Fig. 11. Sequential protection tripping (grounded three phase SLF) – Fault currents at the faulted feeder are lower (approximately 25 kA) prior to tripping.

Detail simulation results, however, show that the present GIS circuit breakers at Substation Y, could not be safely operated without high risk of re-ignition and re-striking occuring, even when sequential tripping scheme is used. Nonetheless, the SLF for single phase to ground faults was observed not to give high risk of exceeding the imposed envelope of Test Duty 4.

The following Fig. 12 through Fig. 15 are several waveforms showing TRV exceeding the IEC 56 Test Duty 4 envelope:

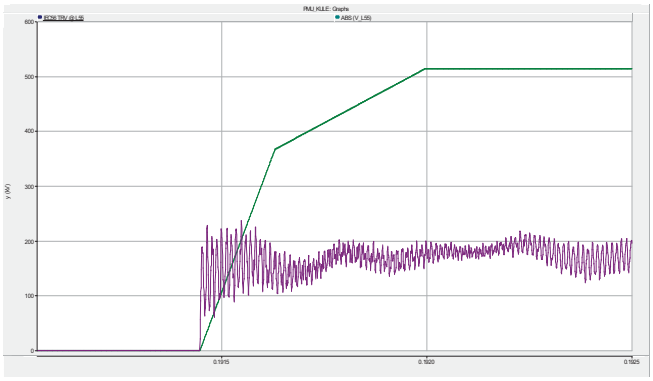

Fig. 12. Conventional protection tripping (grounded three phase SLF) – Voltage across last pole to open for faulted feeder circuit breaker versus IEC56 Test Duty 4 envelope.

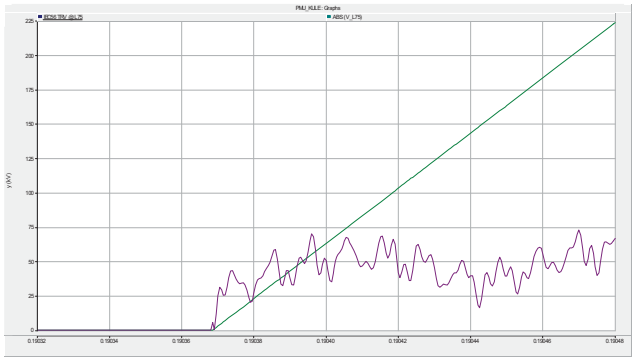

Fig. 13. Sequential protection tripping (grounded three phase SLF) – Voltage across last pole to open for faulted feeder circuit breaker versus IEC56 Test Duty 4 envelope.

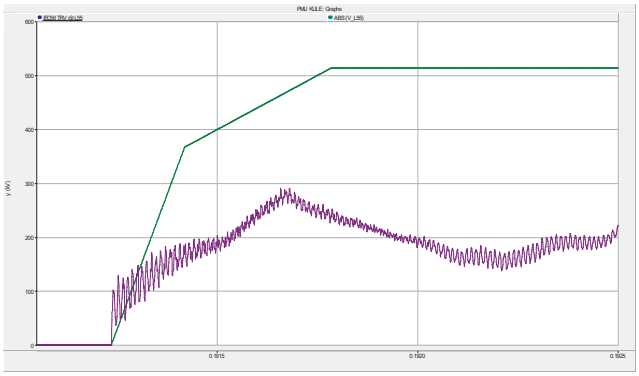

Fig. 14. Conventional protection tripping (ungrounded three phase SLF) – Voltage across last pole to open for faulted feeder circuit breaker versus IEC56 Test Duty 4 envelope.

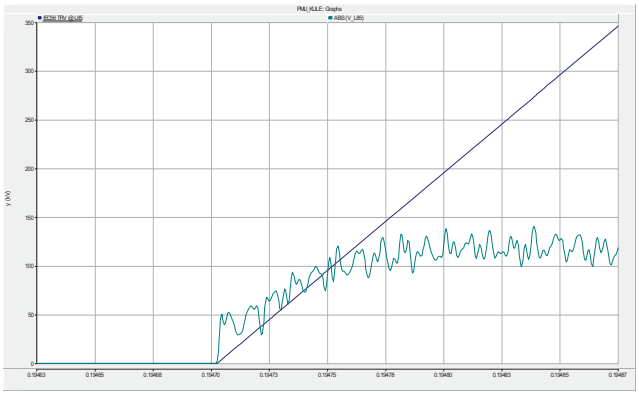

Fig. 15. Sequential protection tripping (ungrounded three phase SLF) – Voltage across last pole to open for faulted feeder circuit breaker versus IEC56 Test Duty 4 envelope.

VII. DISCUSSION

There are numerous factors that influence prospective system TRV of circuit breakers during fault clearance sequence, particularly involving GIS substations.

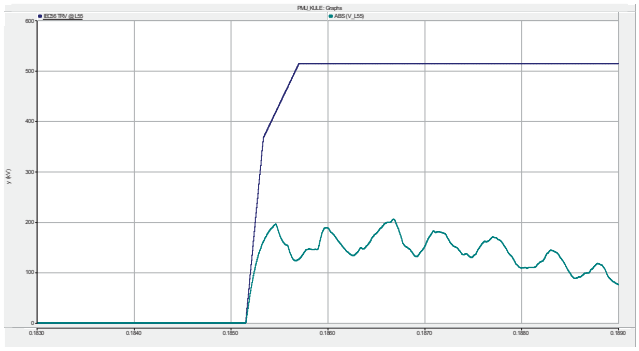

Fig. 16. Conventional protection tripping (grounded single phase SLF) – Voltage across single pole of faulted feeder circuit breaker versus IEC56 Test Duty 4 envelope.

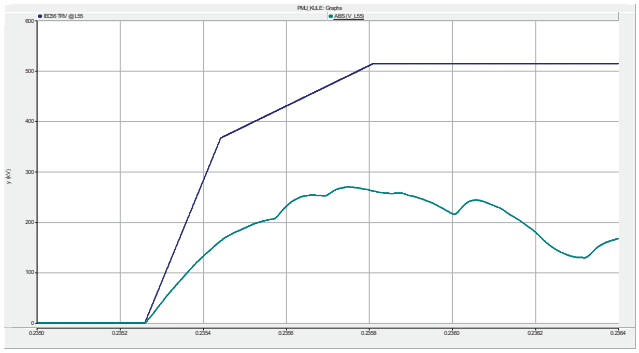

Fig. 17. Sequential protection tripping (grounded single phase SLF) – Voltage across single pole of faulted feeder circuit breaker versus IEC56 Test Duty 4 envelope.

A. Circuit Breaker Design and Specifications

Generally, the breaker itself does not directly contribute to the prospective TRV. The TRV is a function of nearby surge impedance, as well as other system elements. However, for three-phase circuit breakers, spread of pole operation separation times is important for low frequency and slow front transients. In addition, SF6 gas insulated breakers also typically exhibit current chopping level of only a few amperes. Chopping level presents an abrupt disruption to the current flow, i.e. the larger the chopping level the severe the transient it produces.

B. Fault Type and Location

The worst type of fault with respect to producing severe TRV is three-phase symmetrical ungrounded terminal faults, i.e. across the first circuit breaker's pole clearing fault. In term of fault location, it is widely accepted that SLF tends to produce the most extreme voltage recovery conditions. This is due to the line side recovery voltage that appears as a saw-tooth travelling wave. Consequently, it generates a steep initial ramp of voltage that causes severe stresses which may exceed the withstand capability of the insulating medium[19]. The rate-of-rise-of-voltage (RRRV) is also affected by the magnitude and rate-of-change of fault current being interrupted by the circuit breaker[20]. Furthermore, the instant of fault

inception determines the maximum magnitude of fault current to be interrupted by the circuit breaker, i.e. affecting RRRV.

C. Electrical Parameters of Nearby Circuit Elements

As discussed in Reference [19], the slope of Initial TRV (ITRV), significantly depends on the surge impedance of the bus and rate-of-change of current (current transient) being interrupted by the circuit breaker. Capacitances on the source side of circuit breakers will produce slower rate-of-rise of TRV. On the other hand, TRV is less influenced by the natural frequency of nearby transformers.

VIII. CONCLUSION

On the onset, sequential tripping scheme was an attractive proposition as high fault current countermeasure at Substation Y. The steady state and transient stability study results show that the scheme can be applied in Substation Y. However, the electromagnetic transient study findings indicated that successive switching operation of the GIS at Substation Y will give rise the TOV level of unacceptable risk. Thus, the sequential tripping scheme is technically not feasible to be implemented in Substation Y. As a step forward, TNB is working closely with the original equipment manufacturer (OEM) to explore other option such as part replacement, or upgrading of underrated equipment in Substation Y. Nonetheless, sequential tripping scheme is still being consider as one of the plausible high fault current countermeasures, particularly in the case of conventional air insulated switchgear (AIS).

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